SN74LS73N

■ Product Introduction

The SN74LS73N integrates two sets of JK flip-flops triggered by descent edge. Each JK flip-flop has a clear "0" function input (CLR).

■ Product Features

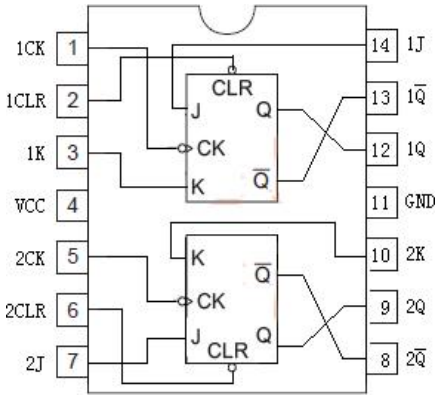
- Integrating 2 sets of JK triggers
- Fully compatible with TTL/DTL input and output logic level
- With clear "0" function input terminal (CLR)
- Package : DIP14, SOP14

■ Product Applications

- Digital logic driver
- Industrial control applications
- Other application areasBattery-powered equipment

■ Package and Pin Assignment

SOP14 or DIP14.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input 1CK	14	Input 1J
2	Input 1CLR	13	Output 1$\overline{Q}$
3	Input 1K	12	Output 1Q
4	Supply VCC	11	Supply GND
5	Input 2CK	10	Input 2K
6	Input 2CLR	9	Output 2Q
7	Input 2J	8	Output 2$\overline{Q}$

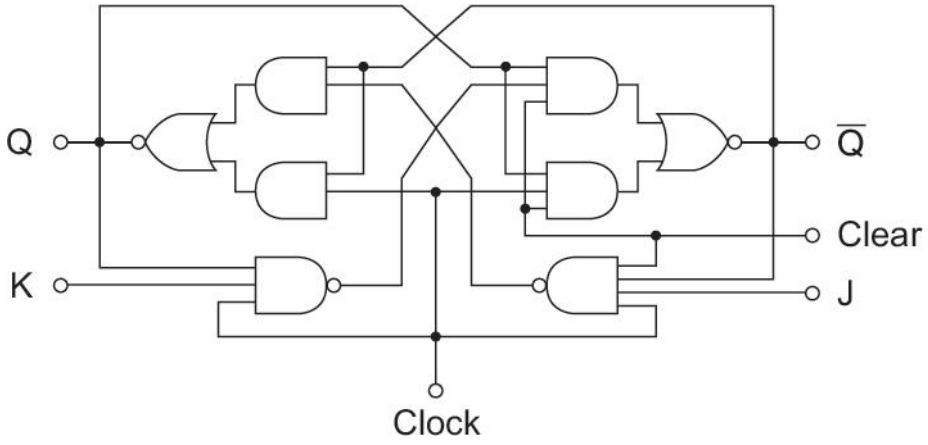


■ Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
welding temperature	T_W	260	℃,10s

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

Block Diagram



Function Table

Inputs				Outputs	
Clear	**Clock**	**J**	**K**	**Q**	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Qo	$\overline{Q}$o
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Qo	$\overline{Q}$o

H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,

Q_0; level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$; complement of $\overline{Q}_0$ or level of Q before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

Recommended Operating Conditions

Item		Symbol	Min	Tpy	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	uA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	0		60	℃
Pulse width	CK(Clock High)	t_w	50	—	—	ns
	CLR(Clear Low)	t_w	50	—	—	
Setup time	"H"Data	t_{su}	50↓	—	—	ns
	"L"Data	t_{su}	50↓	—	—	
Hold time		t_h	0↓	—	—	ns

Note: ↓: The arrow indicates the falling edge.

Electrical Characteristics (T_A=25℃, Unless specified)

Item		Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage		V_{IH}	2	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	3.5	—	V	I_{OH}=-400uA	VCC=4.75V, V_{IL}=0.8V
		V_{OL}	—	0.15	0.4	V	I_{OL}=4mA	VCC=4.75V,V_{IH}=2V
			—	0.28	0.5		I_{OL}=8mA	
Input current	J、K	I_{IH}	—	0.1	20	uA	VCC=5.25V, V_I=2.7V	
	Clear		—	0.1	60			
	Clock		—	0.1	80			
	J、K	I_{IL}	—	0.1	-0.4	mA	VCC=5.25V, V_I=0.4V	
	Clear		—	0.1	-0.8			
	Clock		—	0.1	-0.8			
	J、K	I_I	—	0.1	100	uA	VCC=5.25V, V_I=7V	
	Clear		—	0.1	300			
	Clock		—	0.1	400			
Short-circuit output current *		I_{OS}	-20	-35	-100	mA	VCC=5.25V	
Supply current **		I_{CC}	—	2.7	6	mA	VCC=5.25V	
Input clamp voltage		V_{IK}	—	0.9	-1.5	V	VCC=4.75V, I_I =−18mA	

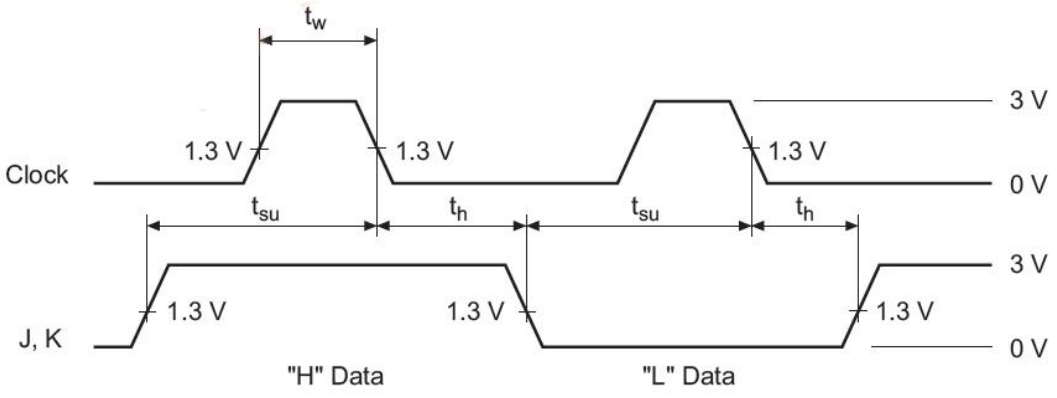
Note1: *only one output port is short circuited each time, and the short circuit time is not more than one second.

Note 2：**With all outputs open, I_{CC} is measured with the Q and Q outputs high in turn. At time of measurement, the clock input is founded.

Switching Characteristics (T_A=25℃, Unless specified)

Item	Symbol	Input	Output	Min	Tpy	Max	Unit	Conditions
Propagation delay time	t_{PLH}	Clear Clock	Qo、$\overline{Q}$o	—	13	—	ns	V_{CC}=5V,C_L=15pF , R_L=2KΩ
	t_{PHL}			—	25	—	ns	

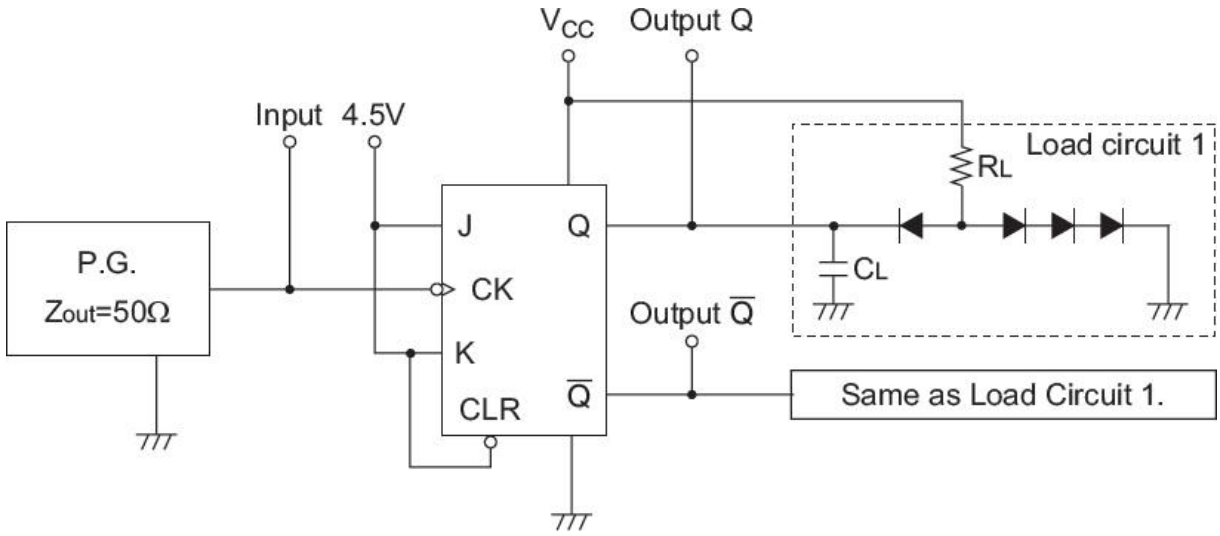
Timing Definition



■ Testing Method

1、t_{PLH}、t_{PHL} (Clock→Q, $\overline{Q}$)

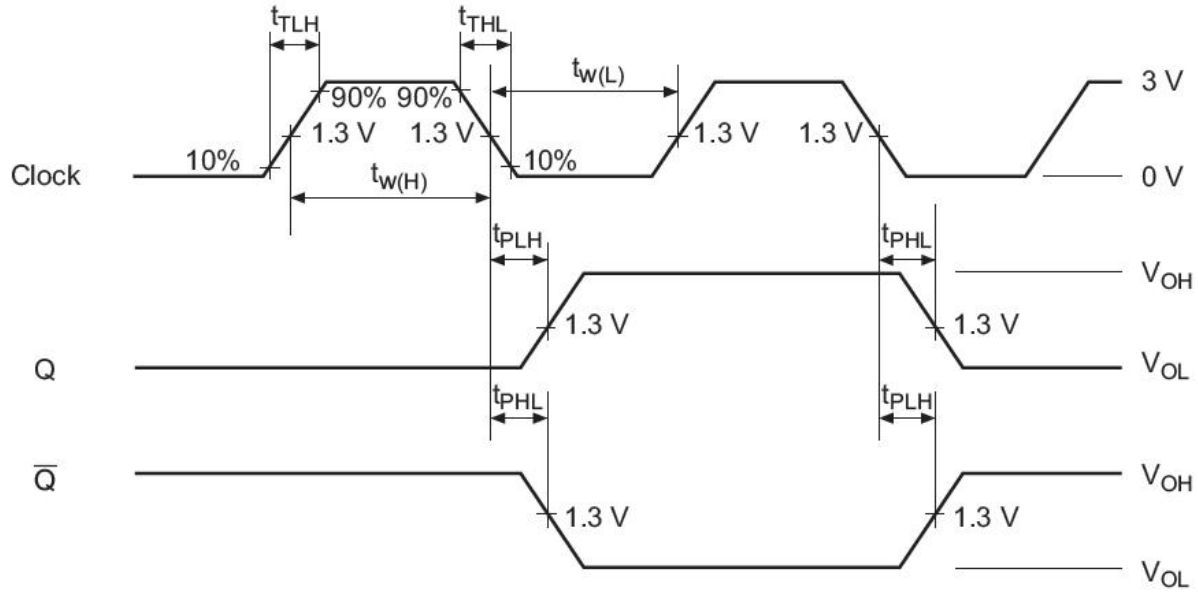
Test Circuit：



Notes:

1. Only one trigger is tested at a time.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. All diode models are 1S2074 (H).

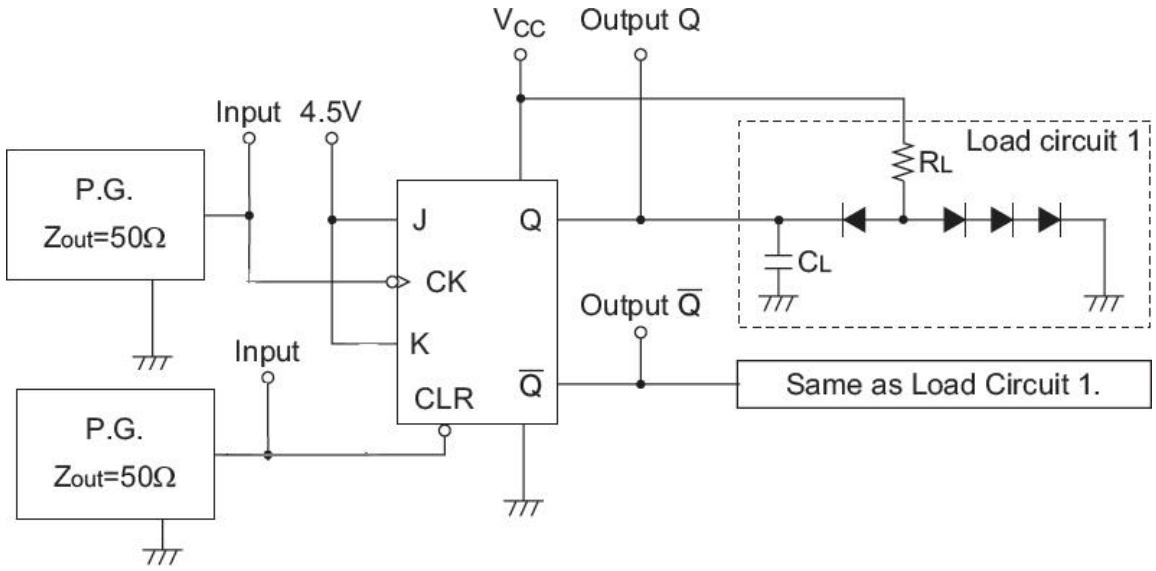
Waveform：



Note：Clock input pulse； $t_{TLH}=t_{THL}=20$ ns， PRR = 1 MHz， duty cycle = 50% 。

2、t_{PHL} (Clear→Q), t_{PLH}(Clear→$\overline{Q}$)

Test Circuit：



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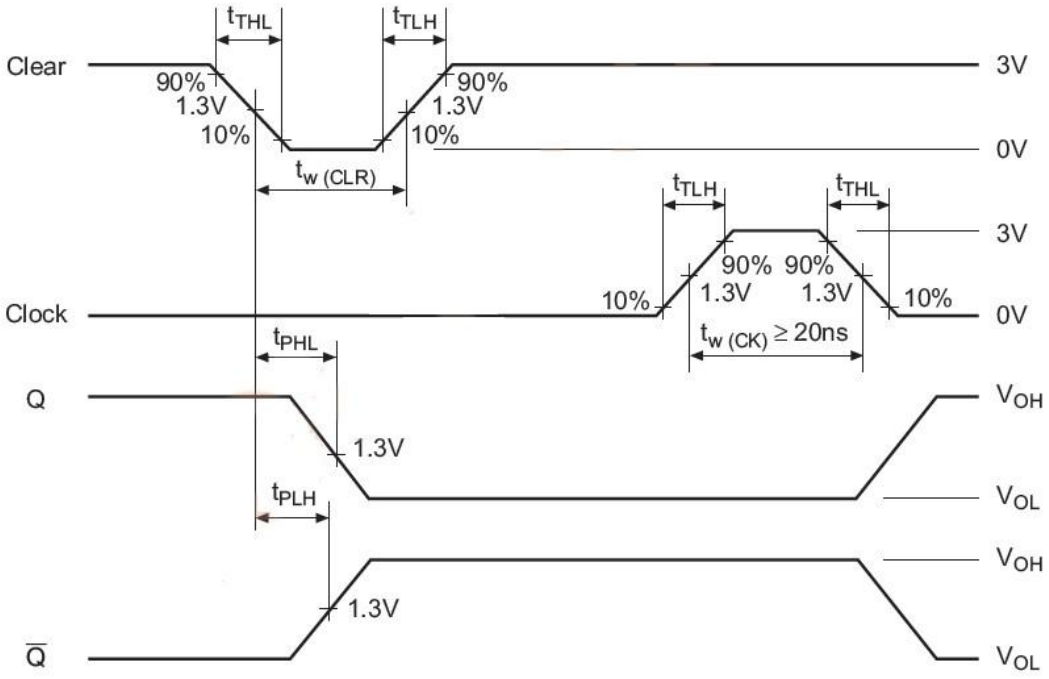
Waveform：

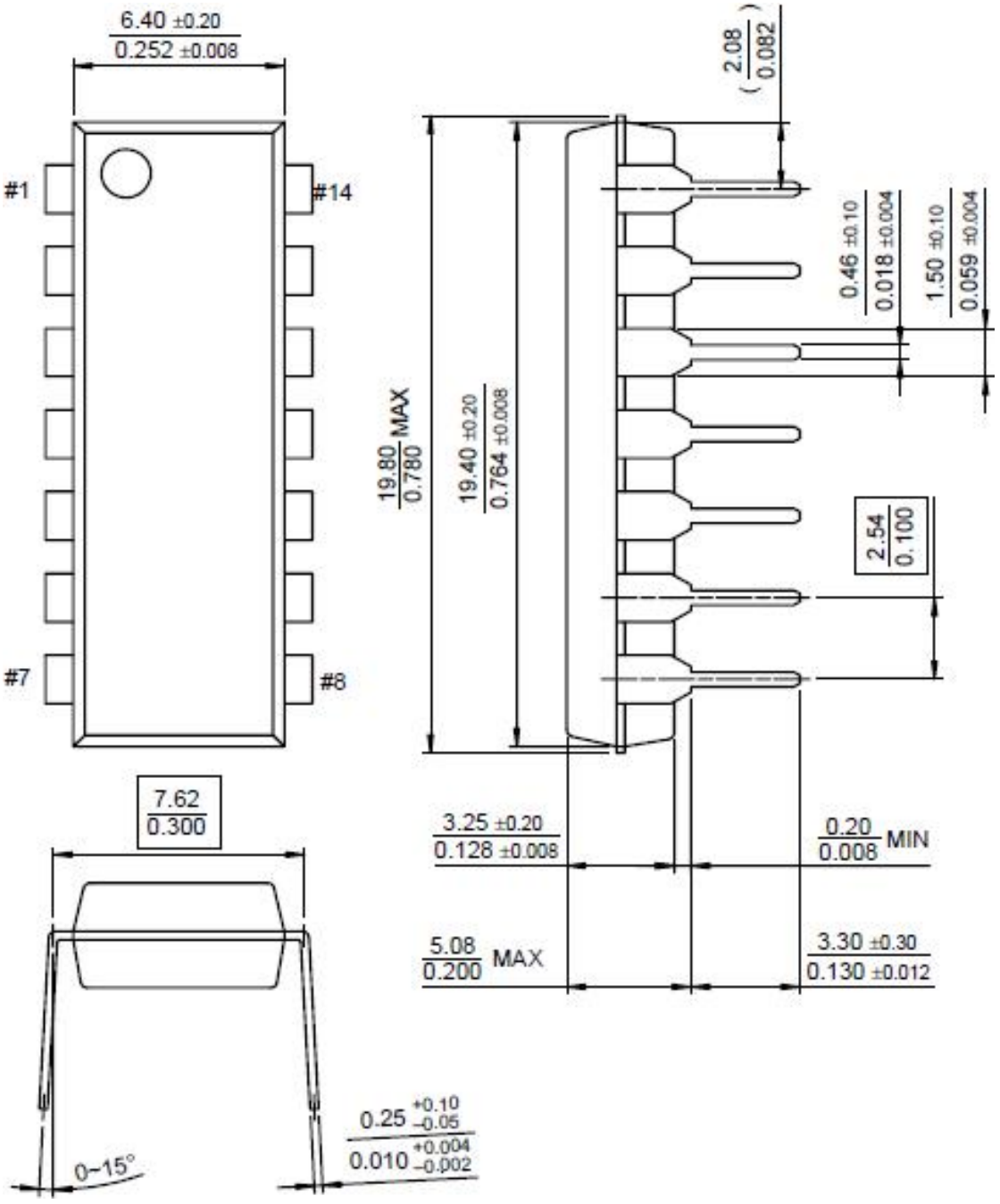


Note： Crear and clock input pulse； t_{TLH} =t_{THL}=20 ns， PRR = 1 MHz， duty cycle = 50%

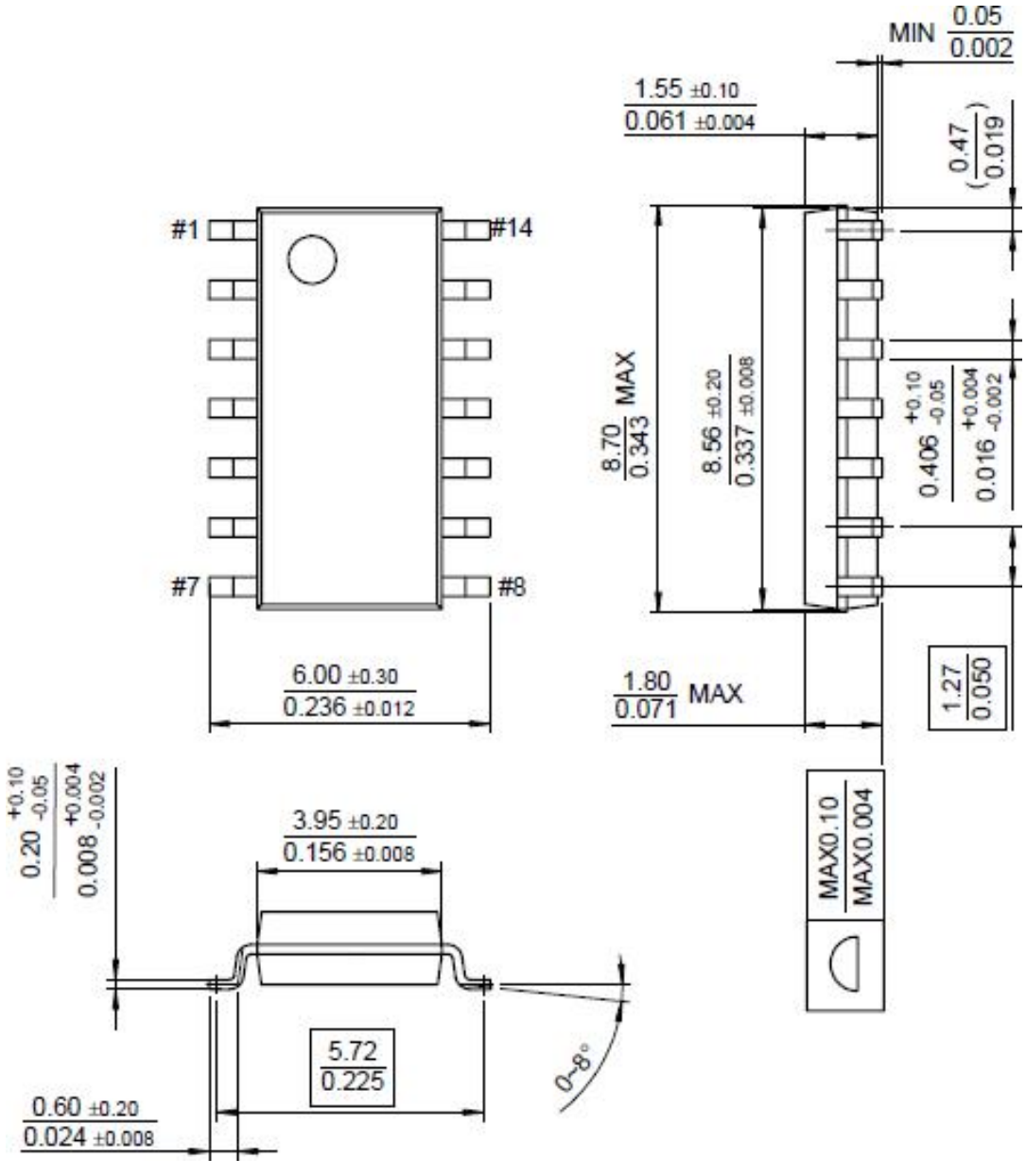
■ Package Dimensions

Unit : mm /inch

DIP14



SOP14


MIN 0.05 0.002
1.55 ±0.10
0.061 ±0.004
0.47 (0.019)
#1
#14
#7
#8
8.70 0.343 MAX
8.56 ±0.20
0.337 ±0.008
+0.10 -0.05
0.406 +0.004 -0.002
0.016
6.00 ±0.30
0.236 ±0.012
1.80 0.071 MAX
1.27 0.050
MAX0.10
MAX0.004
+0.10 -0.05
0.20 +0.004 -0.002
0.008
3.95 ±0.20
0.156 ±0.008
5.72 0.225
0~8°
0.60 ±0.20
0.024 ±0.008